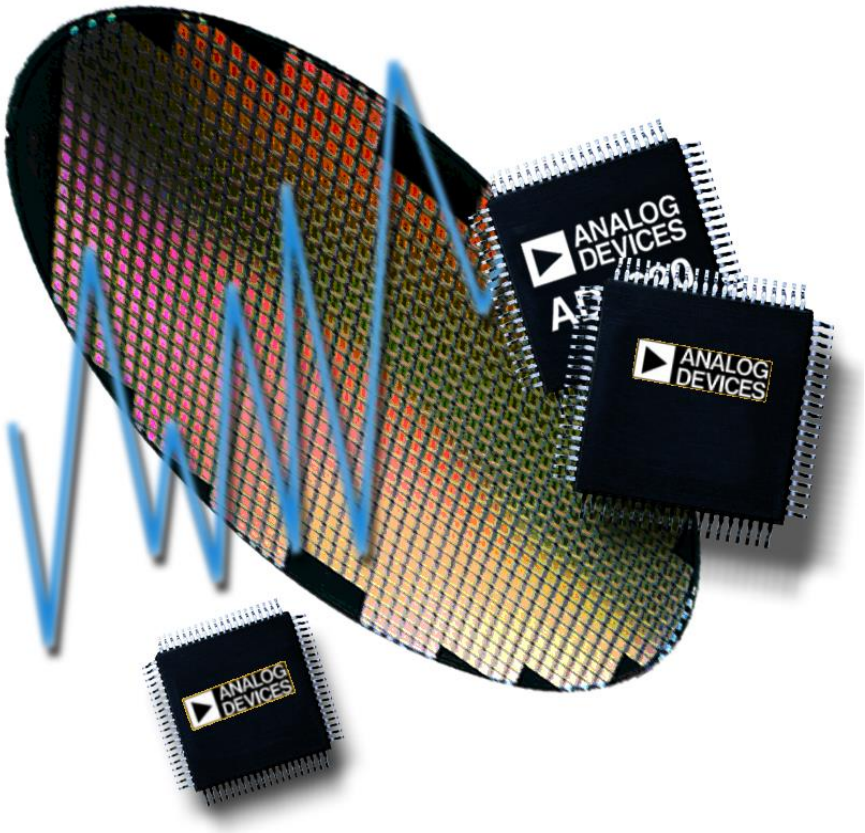

Reliability Report

Report Title: 5x5 LFCSP at JC2 Qualification

Report Number: 19345

Revision: A

Date: 20 April 2022

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the AD9945 product in a 32-LFCSP package at JCET. The AD9945 is a complete analog signal processor for CCD applications. It features a 40 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays.

Table 1: AD9945 Product Characteristics

Die/Fab

Die Id	TMF764 B
Die Size (mm)	2.83 x 2.09
Wafer Fabrication Site	E_TSMC1108
Wafer Fabrication Process	0.35um CMOS
Approximate Transistor Count	30,300
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu(0.5%)

Package/Assembly

Package	32-LFCSP
Body Size (mm)	5.00 x 5.00 x 0.00
Assembly Location	JCET (JC2)
Molding Compound	Sumitomo G700LA
Lead Frame Material	Copper
Lead Finish	NA
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 through 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: LFCSP at JCET (JC2) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	AD9945	Q19345.1.HS1	45	0
Solder Heat Resistance (SHR) [1]	J-STD-020	MSL-3	AD9945	Q19345.1.SH1	11	0
				Q19345.2.SH2	11	0
				Q19345.3.SH3	11	0
Temperature Cycling (TC) [1]	JESD22-A104	-65°C/+150°C, 500 Cycles	AD9945	Q19345.1.TC1	45	0
				Q19345.2.TC2	45	0
				Q19345.3.TC3	45	0
Unbiased HAST (UHST) [1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	AD9945	Q19345.1.UH1	45	0
				Q19345.2.UH2	45	0
				Q19345.3.UH3	45	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Field-Induced Charged Device Model (FICDM) ESD testing is summarized in Table 3. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 3: AD9945 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	32-LFCSP	JS-002	1Ω, Cpkg	±1250V	±0V	NA

Approvals

Reliability Engineer: Pernell Marc Mosuela

Additional Information

Data sheets and other additional information are available on Analog Devices' web site